In the Claims:

Claims 1-8 (canceled)

Claim 9 (currently amended): An FDSOI device comprising:

a bulk semiconductor substrate having a top surface, a buried oxide layer atop said top surface of said substrate and a thin undoped ~~SOI~~ SOI silicon layer atop said buried oxide layer thereon, said buried oxide layer having a thickness in the range between 50 and 60 nm, and said ~~SOI~~ SOI silicon layer having a top surface and having a thickness in the range between 5 and 20 nm;

a doped gate poly feature on said top surface of said ~~SOI~~ SOI silicon layer, said doped gate poly feature having a length in the range between 40 and 75 nm, said doped gate poly feature having outer sidewalls, said doped gate tapered polysilicon features each having a base and a top, each said base being wider than said top, each said tapered polysilicon feature having a tapered surface connecting said poly feature comprising a first and a second tapered polysilicon feature having a gap therebetween, said first and second base to said top opposite said outer sidewalls, said tapered surfaces being at an angle with respect to said top surface of said bulk substrate, said gap having a bottom edge, said bottom edge of said gap being a portion of said top surface of said ~~SOI~~ SOI silicon layer and said bottom edge of said gap having a length;

said doped gate poly feature has a pair of extension implanted regions in said ~~SOI~~ SOI silicon layer, said extension implanted regions extending under said first and second tapered polysilicon features;

said doped gate poly feature has a pair of dielectric spacers abutting said gate poly feature outer sidewalls, said dielectric spacers having a top and a bottom; and

source/drain implanted regions in said ~~SOI~~ SOI silicon layer, said source/drain implanted regions extending under said dielectric spacers.

Claim 10 (currently amended): The device of claim 9 further comprising:

a layer of cobalt silicide atop a portion of said ~~SOI~~ SOI silicon layer not under said gate poly feature or said dielectric spacers; and

a TEOS layer atop said cobalt silicide layer, said TEOS layer having a thickness in the range between 150 and 200 nm, said TEOS layer having a top surface, said top surface of said TEOS layer being substantially even with said top of said dielectric spacers.

Claims 11-16 (canceled)

Claim 17 (currently amended): A bulk semiconductor substrate having a top surface, a buried oxide layer atop said top surface of said substrate and an undoped SOI silicon layer atop said buried oxide layer thereon, said buried oxide layer having a

thickness in the range between 30 and 80 nm, and said SOI silicon layer having a top surface and having a thickness in the range between 2 and 40 nm; said SOI silicon layer including an SOI structure, said SOI structure comprising:

~~A Silicon-On-Insulator (SOI) structure comprising~~:

a MOS structure including a ploysilicon gate;

dielectric spacers abutting sidewalls of said ploysilicon gate;

tapered poly spacers separated by a gap, wherein said tapered poly spacers are formed by taper-etching said ploysilicon gate;

a gate dielectric in said gap; and

a metal on said gate dielectric and in said gap.

Claim 18 (previously presented): The SOI structure of claim 17, wherein said metal forms a metal gate, and wherein said metal gate is less than 50 nm in length.

Claim 19 (previously presented): The SOI structure of claim 17, wherein said taper-etching uses Reactive Ion Etching utilizing a mixture of HBr and Cl_2 etch gases.

Claim 20 (previously presented): The SOI structure of claim 17, said taper-etching is achieved by adjusting a temperature to be in a range of 30° C to 70° C, adjusting Cl_2/HBr gas flow ratio to be in a range of 0.5 to 1.5, and adjusting a taper angle to be in a range of 75° to 85°.

Claim 21 (previously presented): The SOI structure of claim 20, wherein said metal forms a metal gate, and wherein said metal gate is less than 50 nm in length.